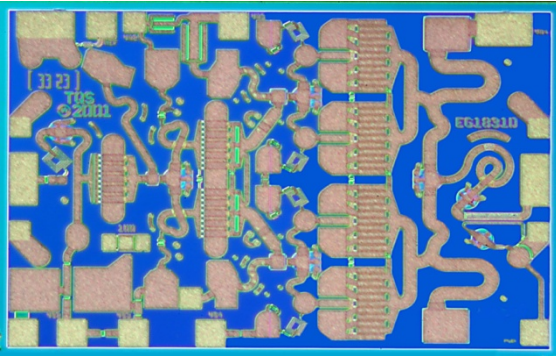


**13 - 17 GHz 2.5 Watt, 25dB Power Amplifier**

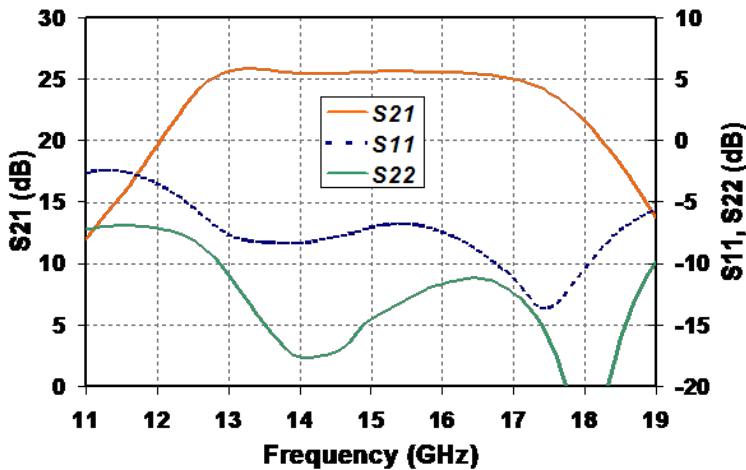


**Key Features and Performance**

- 34 dBm Midband Pout
- 25 dB Nominal Gain
- 7 dB Typical Input Return Loss
- 12 dB Typical Output Return Loss
- Built-in Directional Power Detector with Reference
- 0.25µm pHEMT Technology
- Bias Conditions: 7V, 640mA
- Chip dimensions:  
2.03 x 1.39 x 0.10 mm  
(0.080 x 0.055 x 0.004 inches)

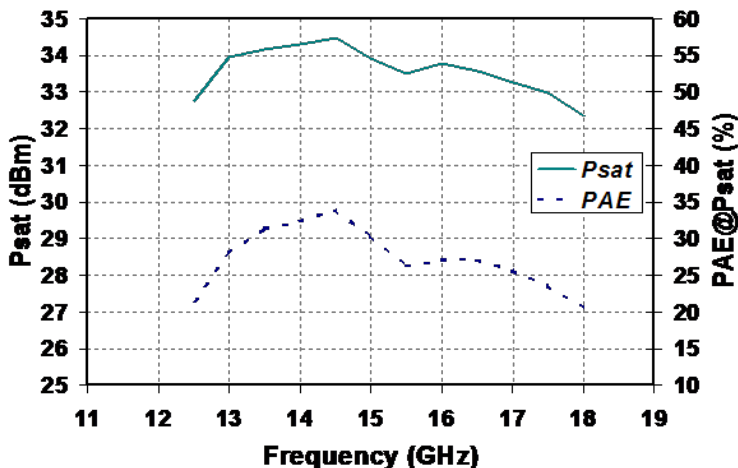
**Preliminary Measured Performance**

Bias Conditions: Vd=7V Id=640mA



**Primary Applications**

- VSAT
- Point-to-Point



Datasheet subject to change without notice

**TABLE I  
MAXIMUM RATINGS**

Symbol	Parameter <u>1/</u>	Value	Notes
V <sup>+</sup>	Positive Supply Voltage	8 V	<u>2/</u>
V <sup>-</sup>	Negative Supply Voltage Range	-5V to 0V	
I <sup>+</sup>	Positive Supply Current (Quiescent)	1300 mA	<u>2/</u>
I <sub>G</sub>	Gate Supply Current	18 mA	
P <sub>IN</sub>	Input Continuous Wave Power	24 dBm	<u>2/</u>
P <sub>D</sub>	Power Dissipation	10.5 W	<u>2/ 3/</u>
T <sub>CH</sub>	Operating Channel Temperature	200 °C	<u>4/ 5/</u>
	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 3/ When operated at this bias condition with a base plate temperature of 70°C, the median life is 2.3E4.
- 4/ These ratings apply to each individual FET.
- 5/ Junction operating temperature will directly affect the device median time to failure (T<sub>m</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

**TABLE II  
DC PROBE TEST  
(T<sub>A</sub> = 25 °C, Nominal)**

NOTES	SYMBOL	LIMITS		UNITS
		MIN	MAX	
<u>1/</u>	I <sub>DSS</sub>	80	381	mA
<u>1/</u>	G <sub>M</sub>	175	425	mS
<u>2/</u>	V <sub>P</sub>	0.5	1.5	V
<u>2/</u>	V <sub>BVGS</sub>	8	30	V
<u>2/</u>	V <sub>BVGD</sub>	13	30	V

- 1/ Measurements are performed on a 800µm FET.
- 2/ V<sub>P</sub>, V<sub>BVGD</sub>, and V<sub>BVGS</sub> are negative.

**TABLE III**  
**RF CHARACTERIZATION TABLE**  
 (T<sub>A</sub> = 25°C, Nominal)  
 (V<sub>d</sub> = 7V, I<sub>d</sub> = 640mA ±5%)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS	UNITS
			TYP	
Gain	Small Signal Gain	F = 13 – 17 GHz	25	dB
IRL	Input Return Loss	F = 13 – 17 GHz	7	dB
ORL	Output Return Loss	F = 13 – 17 GHz	12	dB
PWR	Output Power @ Pin = +15 dBm	F = 13 – 17 GHz	34	dBm

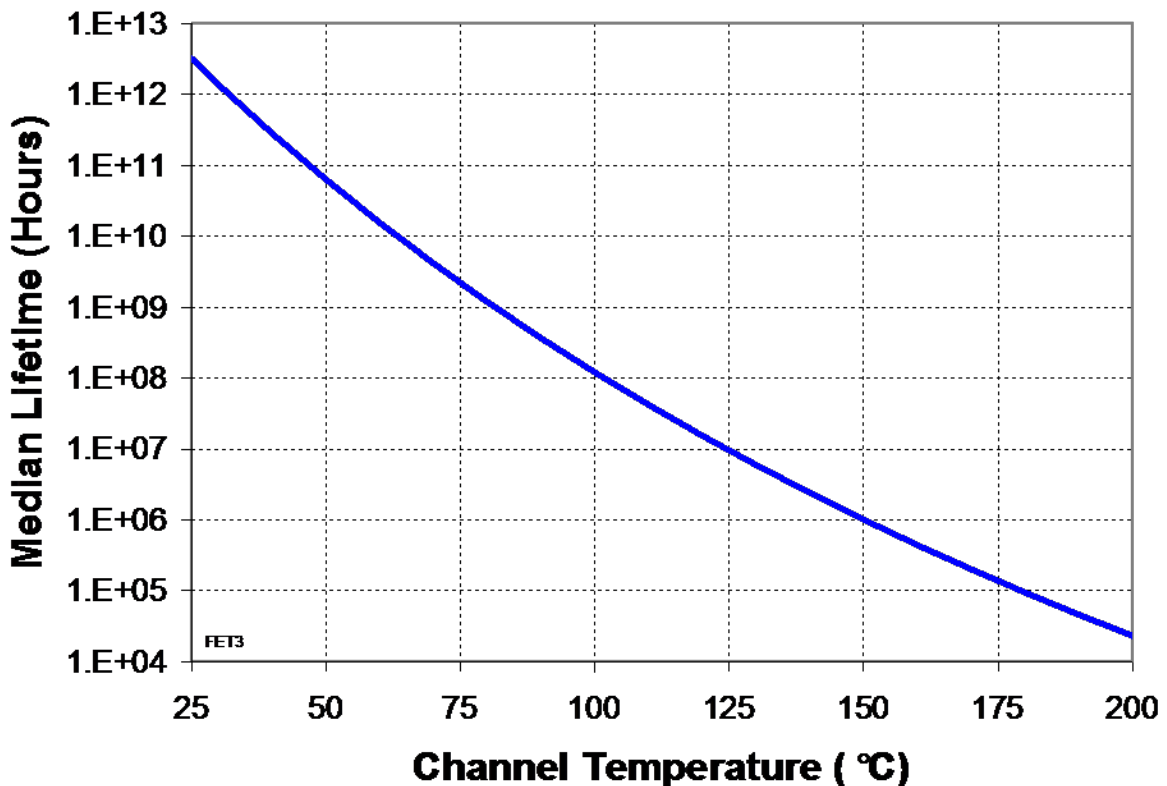
Note: Table III Lists the RF Characteristics of typical devices as determined by fixtured measurements.

**TABLE IV  
THERMAL INFORMATION**

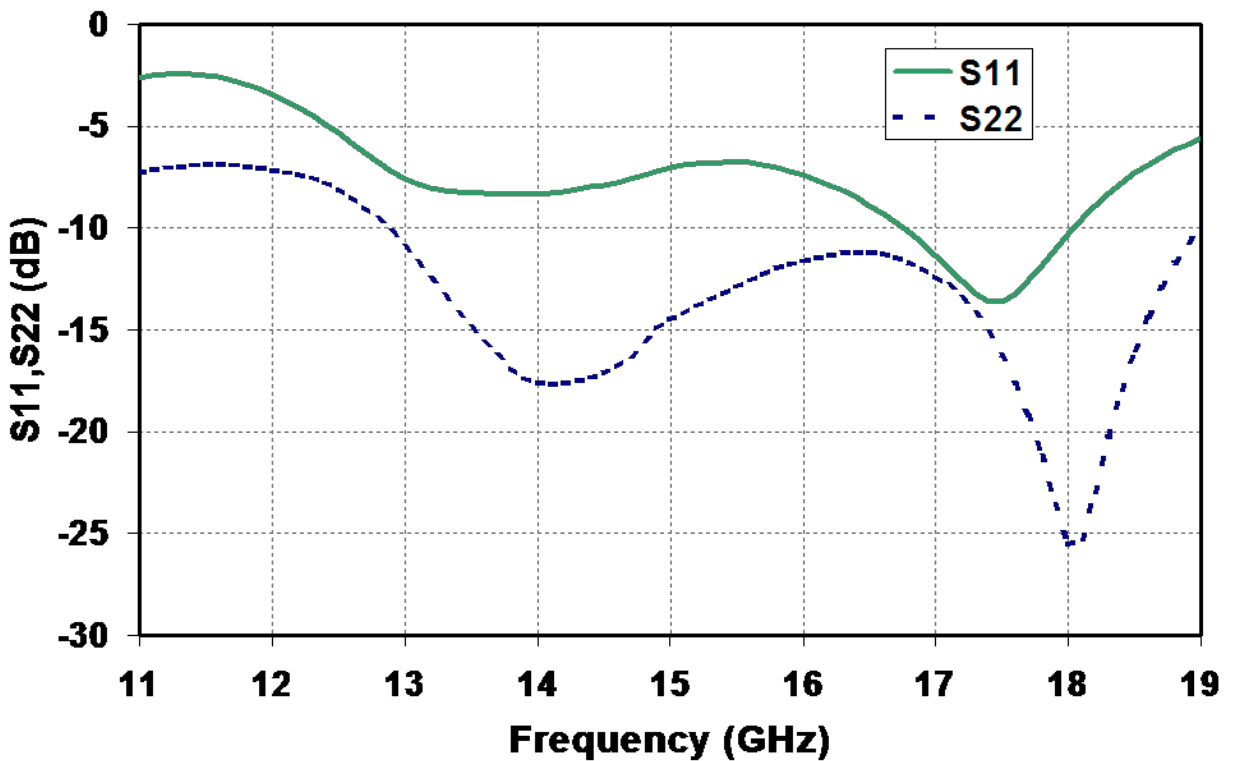
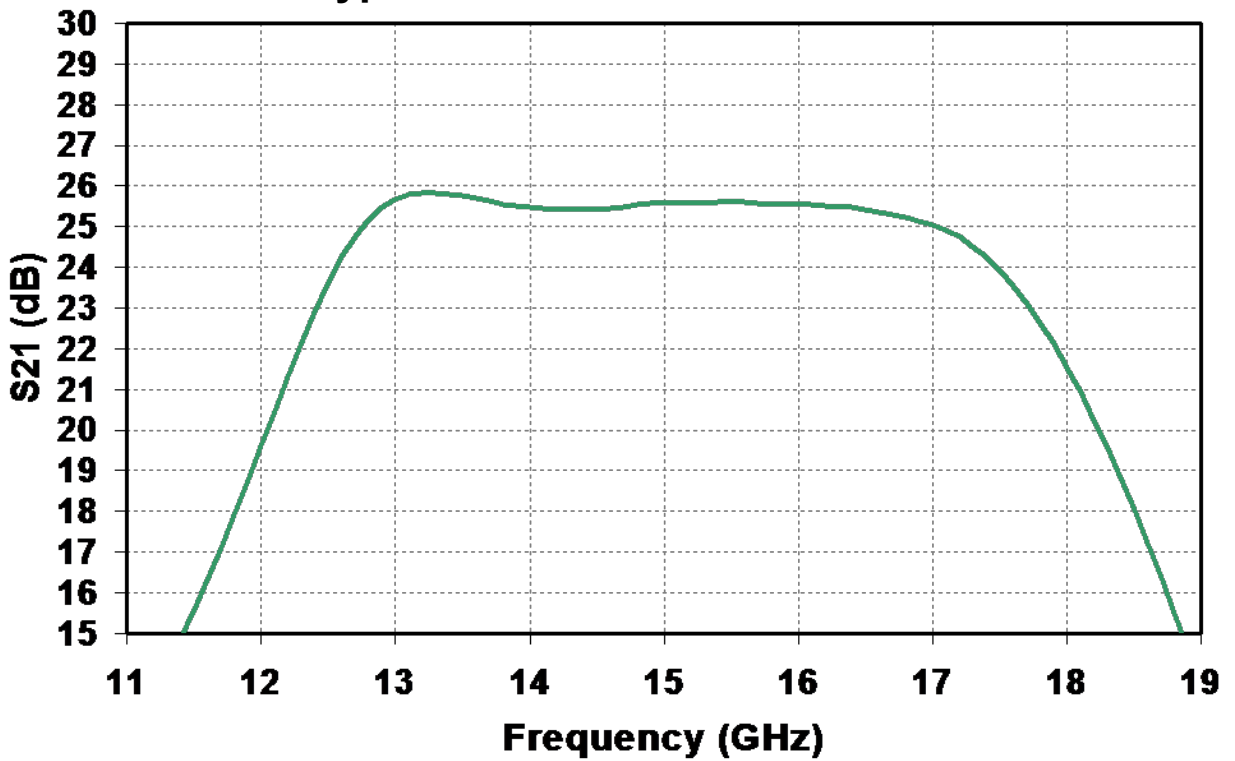
PARAMETER	TEST CONDITION	T <sub>CH</sub> (°C)	θ <sub>JC</sub> (°C/W)	T <sub>m</sub> (HRS)
θ <sub>JC</sub> Thermal Resistance (Channel to Backside)	V <sub>D</sub> = 7V I <sub>D</sub> = 640mA P <sub>D</sub> = 4.48W	125.7	12.44	8.9E+6

Note: Assumes eutectic attach using 1.5mil 80/20 AuSn mounted to a 20mil CuMo carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

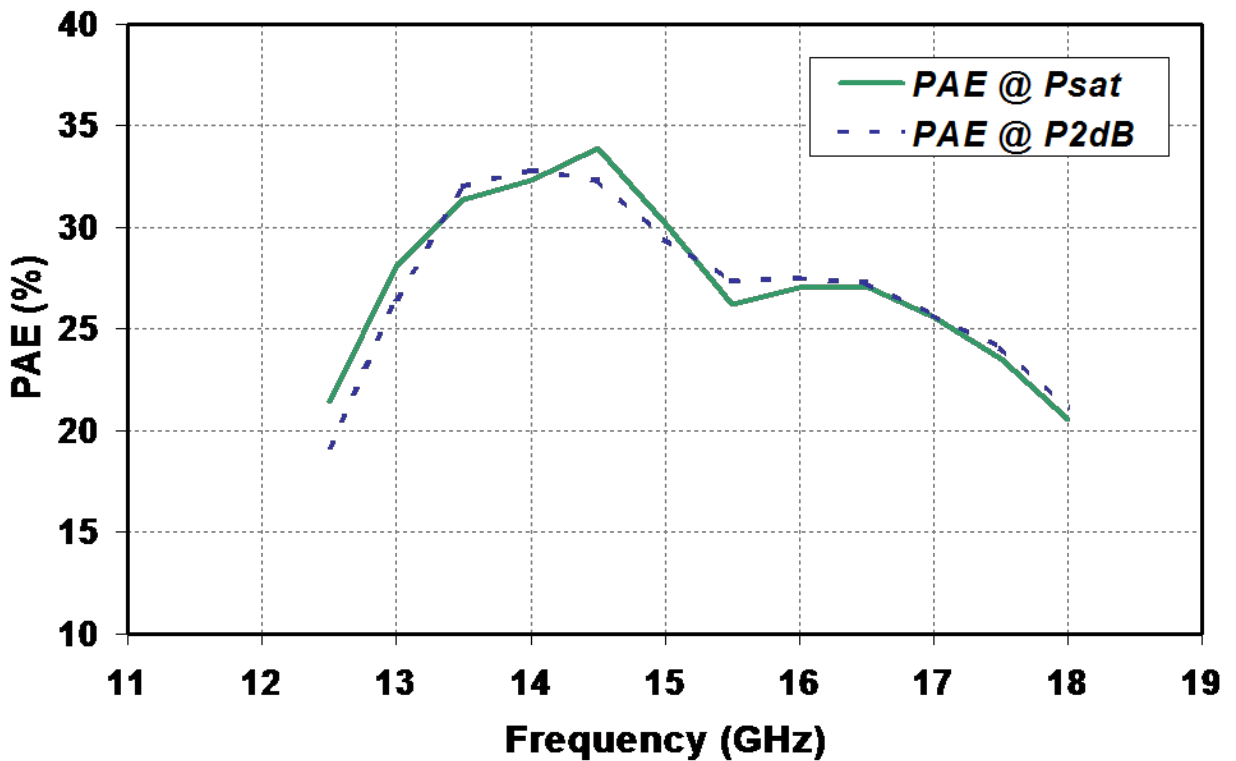
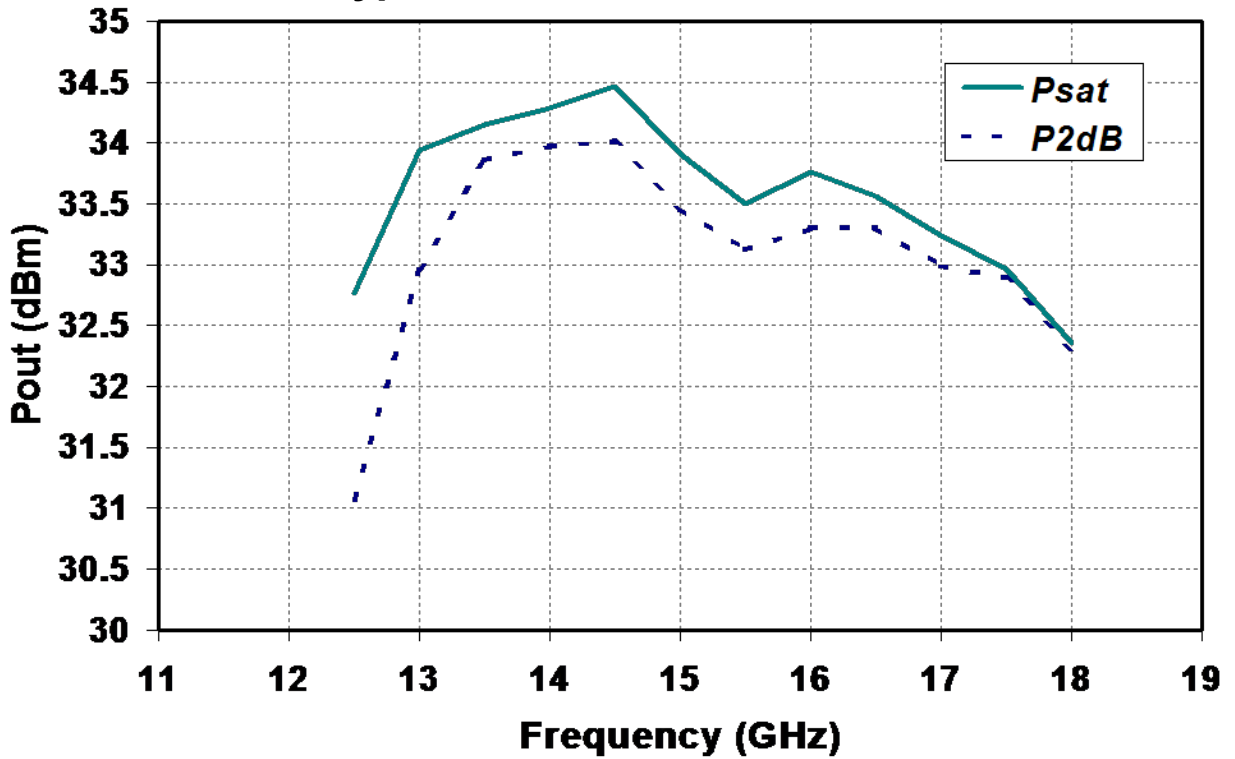
**Median Lifetime (T<sub>m</sub>) vs. Channel Temperature**



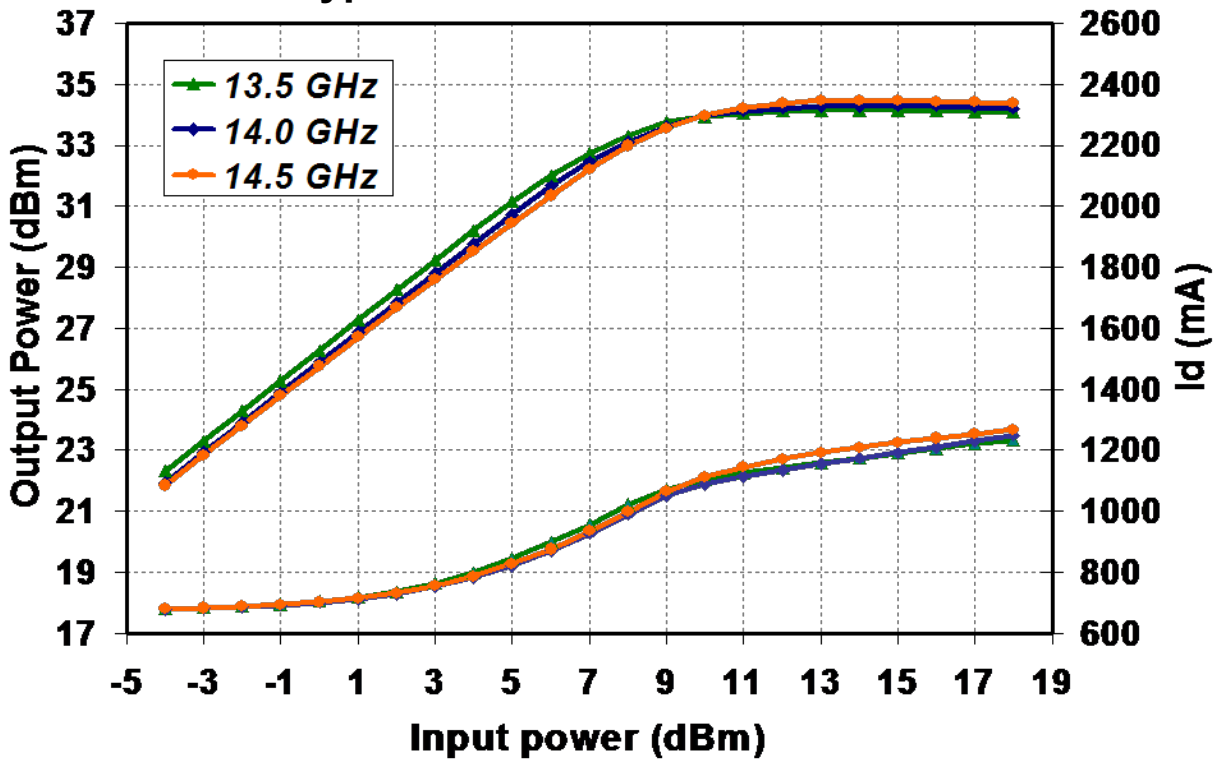
**Typical Fixtured Performance**



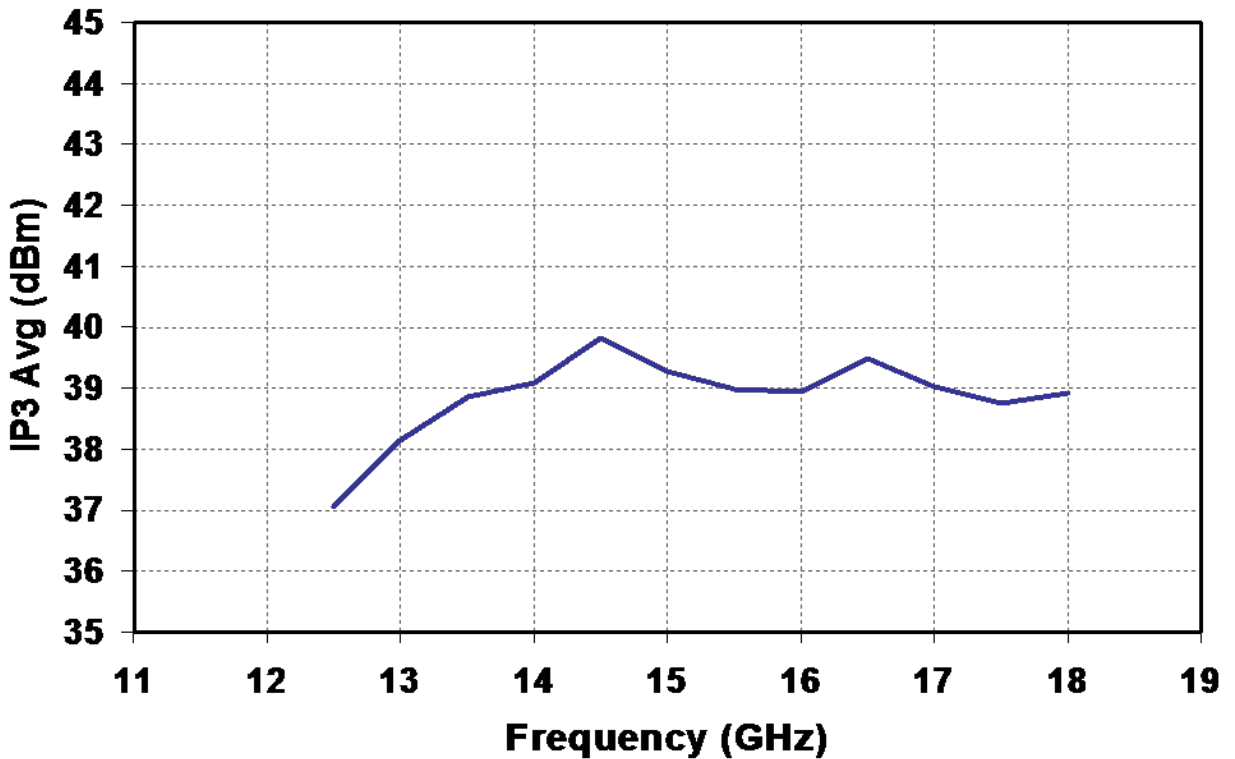
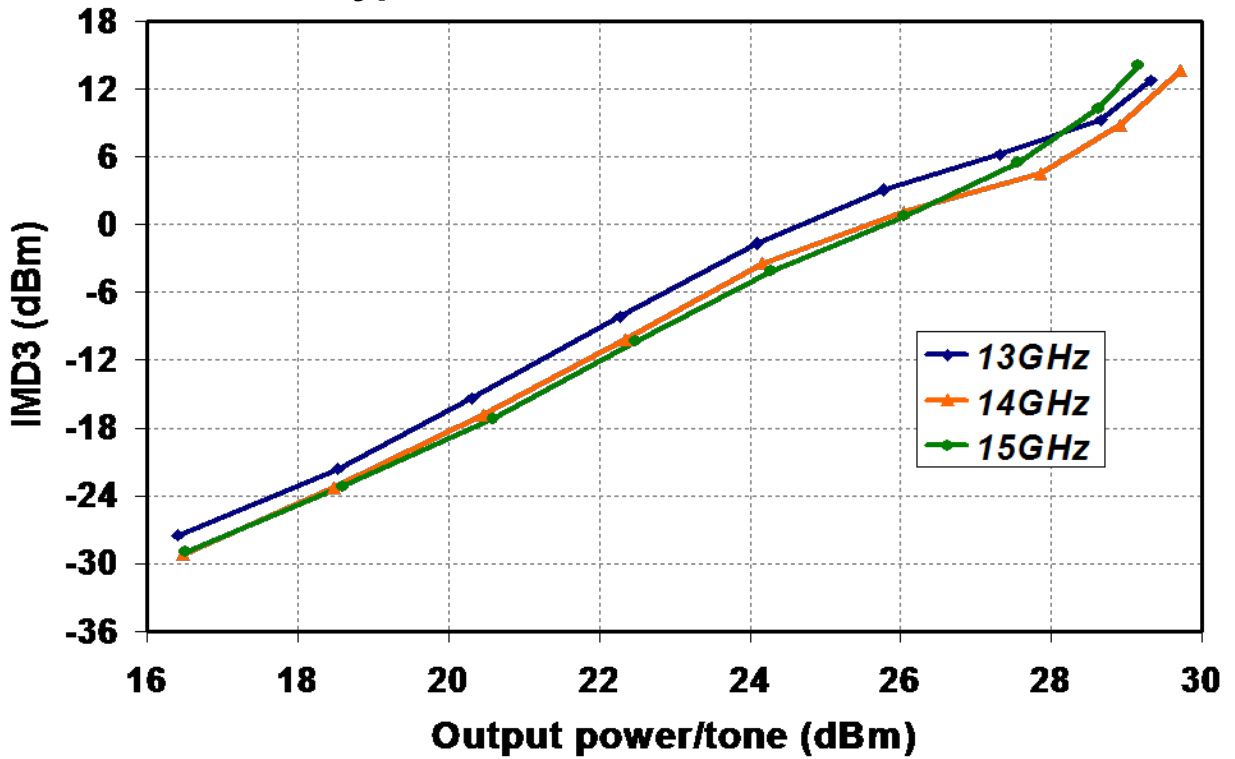
**Typical Fixtured Performance**



**Typical Fixtured Performance**

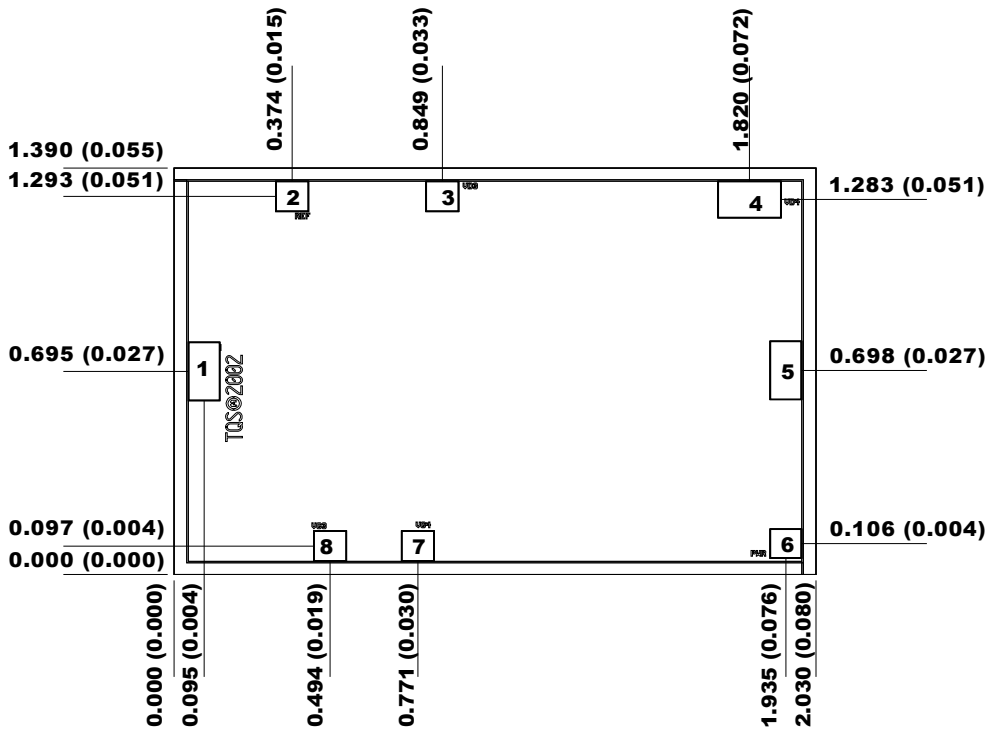


**Typical Fixtured Performance**





**Mechanical Drawing**



**Units: millimeters (inches)**

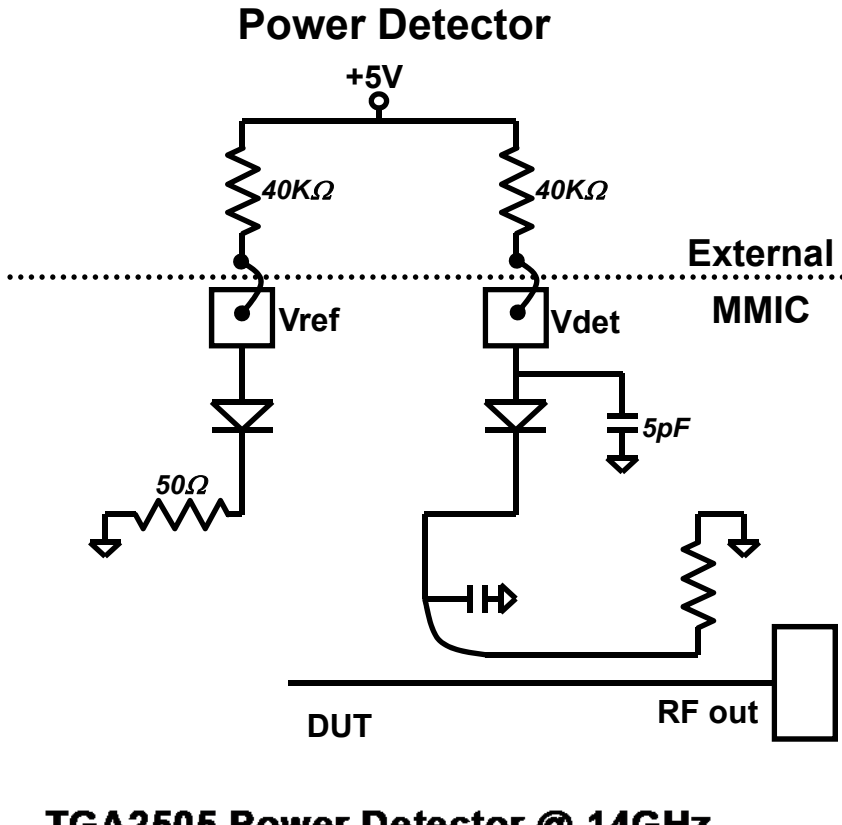
**Thickness: 0.100 (0.004)**

**Chip edge to bond pad dimensions are shown to center of bond pad**

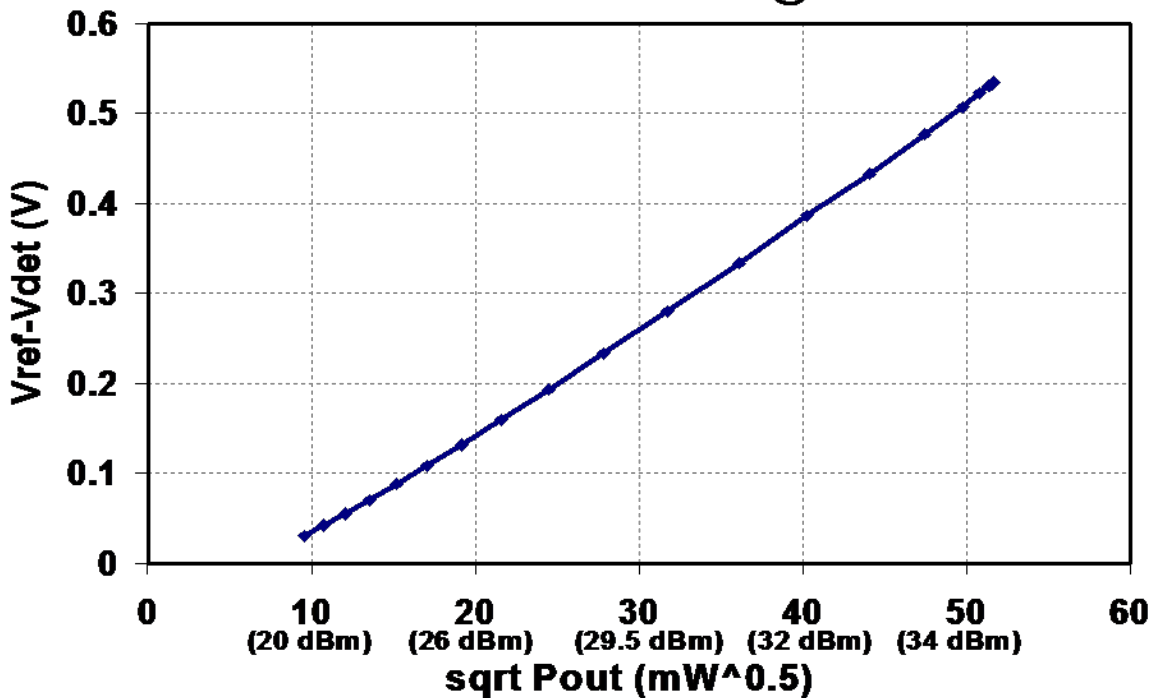
**Chip size tolerance: +/- 0.051 (0.002)**

**GND IS BACKSIDE OF MMIC**

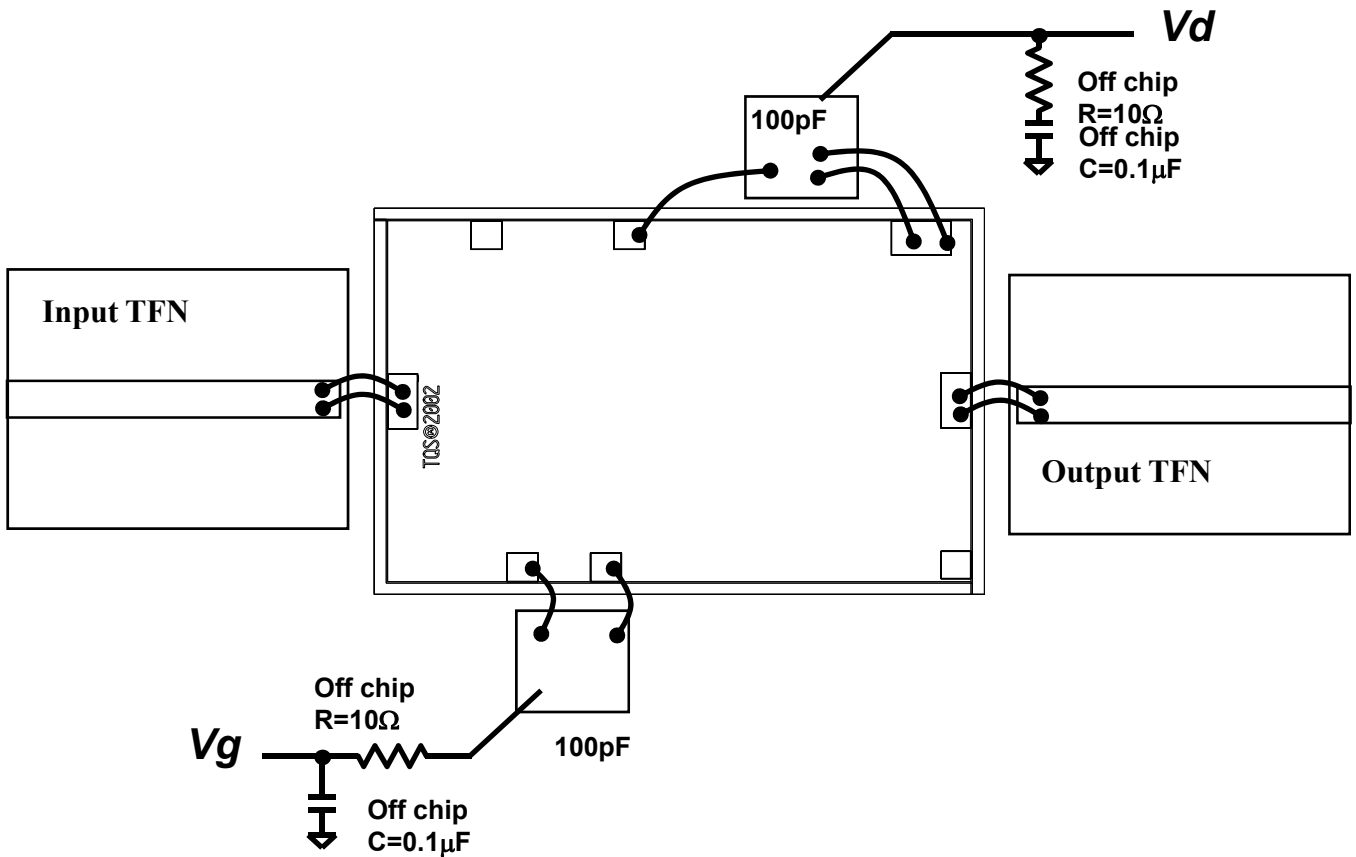
<b>Bond pad #1</b>	<b>(RF Input)</b>	<b>0.100 x 0.200 (0.004 x 0.008)</b>
<b>Bond pad #2</b>	<b>(Vref)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #3</b>	<b>(Vd3)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #4</b>	<b>(Vd4)</b>	<b>0.200 x 0.125 (0.008 x 0.005)</b>
<b>Bond pad #5</b>	<b>(RF Output)</b>	<b>0.100 x 0.200 (0.004 x 0.008)</b>
<b>Bond pad #6</b>	<b>(Vdet)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #7</b>	<b>(Vg4)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #8</b>	<b>(Vg3)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>



**TGA2505 Power Detector @ 14GHz**



**Chip Assembly & Bonding Diagram**



**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

## Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C. (30 seconds maximum)
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***